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[TITLE OF THE INVENTION] RADIO COMMUNICATION APPARATUS AND CODING PROCESSING METHOD

[SCOPE OF CLAIMS FOR PATENT]

[Claim 1] A radio communication apparatus comprising:

first number-of-bits increasing means for increasing the specified number of bits among the number of bits for a Rate matching in data subjected to error correction coding;

interleaving means for rearranging data whose the number of bits is increased; and

second number-of-bits increasing means for increasing remaining the number of bits among the number of bits for the Rate matching in rearranged data.

[Claim 2] The radio communication apparatus according to claim 1, wherein the first number-of-bits increasing means increase the number of bits of the data that is subjected to the error correction coding in accordance with error correction code rate.

[Claim 3] A radio communication apparatus comprising:

number-of-bits increasing means for increasing the number of bits of data subjected to error correction coding in accordance with error correction coding rate; and

interleaving means for rearranging data whose the number of bit is increased.

[Claim 4] A radio communication apparatus comprising:

reception means for receiving data whose the number of bits is increased before and after an interleaving;

first number-of-bits decreasing means for decreasing the number of bits increased after the interleaving in received data;

deinterleaving means for performing inverse rearrangement against the interleaving in data whose the number of bits is decreased; and

second number-of-bits decreasing means for decreasing the number of bits increased before the interleaving in data which is subjected to a deinterleaving.

[Claim 5] A radio communication apparatus comprising:

reception means for receiving data whose the number of bits is increased in accordance with error correction code rate before the data is rearranged;

deinterleaving means for performing inverse rearrangement against an interleaving in received data; and

number-of-bits decreasing means for decreasing the number of bits in data that is subjected to a deinterleaving.

[Claim 6] A radio communication terminal apparatus equipped with a radio communication apparatus described

in any one of claim 1 to claim 5.

[Claim 7] A radio communication base station apparatus equipped with a radio communication apparatus described in any one of claim 1 to claim 5.

[Claim 8] A coding processing method comprising:

the first number-of-bits increasing step of increasing the specified number of bits among the number of bits for a Rate matching in data subjected to error correction coding;

the interleaving step of rearranging data whose the number of bits is increased; and

the second number-of-bits increasing step of increasing remaining the number of bits among the number of bits for the Rate matching in rearranged data.

[DETAILED DESCRIPTION OF THE INVENTION]

[0001]

[Technical Field of the Invention]

The present invention relates to a radio communication apparatus and a coding processing method employed in CDMA radio communication apparatus.

[0002]

[Prior Art]

In CDMA radio communication apparatus, Rate matching processing is performed in order to enhance an effect of error correction, and/or in order to transmit data such as a packet, ISDN and so forth while coupling the data. The Rate matching processing is repetition

processing for increasing the number of bits of data in order to adjust coded data to frame length, or puncturing processing for reducing the number of bits of data in order to adjust coded data to frame length. For instance, in a transmitter side, in the case where the transmitter side causes the number of bits of data to be increased, in a receiver side, the receiver side is required to perform processing of decreasing of the number of bits of data. In this case, since the transmitter side performs repetition, it is possible to enhance effect of error correction in the receiver side.

[0003]

FIG.10 is a block diagram illustrating configurations of a conventional coding processing apparatus in the case where repetition is performed in a transmitter side and a conventional decoding processing apparatus in the case where repetition is performed in a transmitter side. The coding processing apparatus 1 includes a coding section 2, an error correction coding section 3, a repetition section 4, and an interleaving section 5. The decoding processing apparatus 10 includes a deinterleaving section 11, a puncturing section 12, an error correction decoding section 13, and a decoding section 14.

[0004]

In the transmitter side, transmitted data 6 is coded in the coding section 2. This coded data is subjected

to error correction coding processing such as convolutional coding and so forth in the error correction coding section 3 before the number of bits is increased in the repetition section 4. The data after repetition is rearranged in the interleaving section 5. Subsequently, the data is subjected to predetermined modulation processing and radio processing and so forth, before being transmitted from a transmission antenna 7.

[0005]

On the other hand, in the receiver side, a signal received by a reception antenna 15 is subjected to predetermined radio processing and demodulation processing and so forth before inverse rearrangement against the interleaving is performed in the deinterleaving section 11. In this rearranged data, the number of bits which are increased in the transmitter side once are decreased in the puncturing section 12. The data is subjected to error correction by Viterbi decoding and so forth in the error correction decoder 13. This data after error correcting is decoded in the decoder 14. According to the above processing, received data 16 is obtained.

[0006]

FIG.11 is a view showing data arrangement in the case where repetition and interleaving processing are performed with the conventional coding processing apparatus 1 employed. Now, data output from the coding

section 2 is taken to be {D1, D2, D3, D4}. The data is subjected to error correction coding processing with "code rate = 1/2" in the error correction coding section 3. As a result, in cases where D1 becomes d1 and d2, D2 becomes d3 and d4, D3 becomes d5 and d6, and D4 becomes d7 and d8, data input to the repetition section 4 becomes data of 8 bits of {d1, d2, d3, d4, d5, d6, d7, d8}. It should be noted that the number of bits per 1 frame is set to 12 bits. The repetition section 4 is provided with a Rate matching table. Further, a pattern of "0 and 1" is stored in the Rate matching table. The pattern of "0 and 1" causes a distribution of increase of bits within a frame to be even.

[0007]

Now, if the Rate matching table is taken to be {1, 0, 1, 0, 1, 0, 1, 0}, since bits corresponding to "1" are increased, thus d1, d3, d5, and d7 showed by under lines are increased. Accordingly, data after repetition becomes {d1, d1, d2, d3, d3, d4, d5, d5, d6, d7, d7, d8}. Careful observation of the data after repetition reveals that there exist two increased bits and one not increased bit within continuous three bits, thus it is found that a distribution of increase of bits becomes even within a frame.

[0008]

The data after repetition is subjected to interleaving in accordance with for instance an

interleaving pattern ; 12[4[2×2]×3[2×2]]. According to this processing, the data after interleaving becomes {d1, d5, d3, d7, d2, d6, d4, d8, d1, d5, d3, d7}. According to these processing, it is possible to avoid a burst error in a propagation path in some degrees. Accordingly, it is possible to improve bit error rate characteristic in some degrees when the receiver side corrects errors.

[0009]

[Problems to be Solved by the Invention]

However, in the above-described conventional coding processing apparatus, the increased bits caused by repetition are partial to a position within a frame according to an interleaving pattern. For this reason, an effect of the repetition deteriorates remarkably. Consequently, the bit error rate characteristic deteriorates when the receiver side corrects errors.

[0010]

Specifically, for instance, in an interleaving pattern showed in FIG.11, increased bits "d1, d3, d5, d7" are partial to both sides within the frame. Accordingly, in the case where a burst error occurs in a propagation path at portions with not-increased bits "d2, d4, d6, d8", the bit error rate characteristic deteriorates when the receiver side corrects errors.

[0011]

The present invention has been made in consideration of the above-mentioned problem, and object of the present

invention is to provide a radio communication apparatus and a coding processing method in which resistibility to a burst error in a propagation path is high, and the apparatus and method are capable of scheming improvement of communication quality.

[0012]

[Means for Solving the Problem]

The inventor of the present invention notes a cause why the increased bits due to the repetition are partial to a portion within a frame. In the case where the repetition is performed at a time about the whole data before interleaving, the increased bits due to the repetition are partial to a portion within the frame. The inventor finds that the repetition is separated to be performed before and after interleaving in well-balanced condition, so that it is possible to prevent mal-distribution of the increased bits due to the repetition within the frame, and the inventor achieves the present invention.

[0013]

Accordingly, the gist of the present invention is that, roughly half the number of bits increased due to the repetition are increased in accordance with a repetition before interleaving, while remaining the number of bits increased due to the repetition are increased in accordance with a repetition after interleaving.

[0014]

[Embodiments of the Invention]

A radio communication apparatus according to a first aspect of the present invention adopts a configuration comprising first number-of-bits increasing means for increasing the specified number of bits among the number of bits for a Rate matching in data subjected to error correction coding, interleaving means for rearranging data whose the number of bits is increased, and second number-of-bits increasing means for increasing remaining the number of bits among the number of bits for the Rate matching in rearranged data.

[0015]

By this configuration, since repetition is performed at two stages before and after interleaving, it is possible to prevent that the bits increased due to repetition exist while being partial to one position within a frame.

[0016]

The radio communication apparatus according to a second aspect of the present invention, in the first aspect, adopts a configuration wherein the first number-of-bits increasing means increase the number of bits of the data that is subjected to the error correction coding in accordance with error correction code rate.

[0017]

A radio communication apparatus according to a third

aspect of the present invention adopts a configuration comprising number-of-bits increasing means for increasing the number of bits of data subjected to error correction coding depending on error correction coding rate, and interleaving means for rearranging data whose the number of bit is increased.

[0018]

By these configurations, since the repetition is performed while determining increased bits in accordance with the code rate, it is possible to prevent that the repetition is performed repeatedly to a plurality of data after error correction coding, which are generated from the same data before error correction coding, caused by error correction coding processing.

[0019]

A radio communication apparatus according to a fourth aspect of the present invention adopts a configuration comprising reception means for receiving data whose the number of bits is increased before and after an interleaving first number-of-bits decreasing means for decreasing the number of bits increased after the interleaving in received data, deinterleaving means for performing inverse rearrangement against the interleaving in data whose the number of bits is decreased, and second number-of-bits decreasing means for decreasing the number of bits increased before the interleaving in data which is subjected to a deinterleaving.

[0020]

A radio communication apparatus according to a fifth aspect of the present invention adopts a configuration comprising reception means for receiving data whose the number of bits is increased in accordance with error correction code rate before the data is rearranged, deinterleaving means for performing inverse rearrangement against an interleaving in received data, and number-of-bits decreasing means for decreasing the number of bits in data that is subjected to a deinterleaving.

[0021]

By these configurations, it is possible to improve a bit error rate characteristic when error correction decoding is performed to data after bit reduction.

[0022]

A radio communication terminal apparatus according to a sixth aspect of the present invention adopts a configuration wherein the radio communication terminal apparatus is equipped with the radio communication apparatus described in any one of the first aspect to the fifth aspect.

[0023]

A radio communication base station apparatus according to a seventh aspect of the present invention adopts a configuration wherein the radio communication base station apparatus is equipped with the radio

communication apparatus described in any one of the first aspect to the fifth aspect.

[0024]

By these configurations, since which are equipped with a radio communication apparatus capable of lowering bit error rate, it is possible to scheme improvement of communication quality.

[0025]

A coding processing method according to an eighth aspect of the present invention comprises the first number-of-bits increasing step of increasing the specified number of bits among the number of bits for a Rate matching in data subjected to error correction coding, the interleaving step of rearranging data whose the number of bits is increased, and the second number-of-bits increasing step of increasing remaining the number of bits among the number of bits for the Rate matching in rearranged data.

[0026]

By this configuration, since repetition is performed at two stages before and after interleaving, it is possible to prevent that the bits increased due to repetition exist while being partial to one position within a frame.

[0027]

Embodiments of the present invention are explained in detail below with reference to accompanying drawings.

(Embodiment 1)

FIG.1 is a block diagram illustrating a configuration of a coding processing apparatus and a decoding processing apparatus according to the embodiment 1 of the present invention. A coding processing apparatus 100 includes a coding section 101, an error correction coding section 102, a first repetition section 103, an interleaving section 104, and a second repetition section 105, and a decoding processing apparatus 110 includes a first puncturing section 111, a deinterleaving section 112, a second puncturing section 113, an error correction decoding section 114, and a decoding section 115.

[0028]

In the transmitter side, transmitted data 106 is coded in the coding section 101. The coded data is subjected to error correction coding processing such as convolutional coding and so forth in the error correction coding section 102, before being outputted to the first repetition section 103. The data after error correction coding processing is subjected to a first repetition as describe later in the first repetition section 103. The data after the first repetition is rearranged in the interleaving section 104, before being subjected to a second repetition as describe later in the second repetition section 105. The data after the second repetition is subjected to predetermined modulation processing and predetermined radio processing and so

forth thereafter. Then the data is transmitted from a transmission antenna 107.

[0029]

On the other hand, in the receiver side, a signal received by a reception antenna 116 is subjected to predetermined radio processing and predetermined demodulation processing and so forth. The data after predetermined radio processing and predetermined demodulation processing is subjected to a first puncturing which is inverse processing against the second repetition in the first puncturing section 111. The data after the first puncturing is subjected to an inverse rearrangement against the interleaving in the transmitter side in the deinterleaving section 112. This rearranged data is subjected to a second puncturing which is inverse processing against the first repetition in the second puncturing section 113. The data after the second puncturing is subjected to error correction by Viterbi decoding and so forth in the error correction decoding section 114, before being decoded in the decoding section 115. According to the above processing, received data 117 is obtained.

[0030]

Next, there will be described about configuration of the first repetition section 103 while employing the block diagram illustrated in FIG.2. In the first repetition section 103, an input memory section 201

temporary stores therein data being subjected to error correction coding. A parameter storage section 202 stores therein various kinds of parameters necessary for performing repetition. A control section 203 outputs a control signal for performing read/write of data to a memory read/write section 204 based on various kinds of parameters stored in the parameter storage section 202. The memory read/write section 204 reads the data from the input memory section 201 successively, and outputs the data while increasing the number of bits to be targeted bits to an output memory section 205 based on the control signal. The output memory section 205 stores the data output successively from the memory read/write section 204 up to the state where the data for one frame is completed. Then the output memory section 205 outputs the data for one frame at the time when the data for one frame is completed.

[0031]

Further, a configuration of the second repetition section 105 is roughly the same as that of the first repetition section 103. Accordingly, concerning the second repetition section 105, an explanation about the configuration is omitted. There will be explained about only operation in an operation explanation describe later. Furthermore, also configurations of the first puncturing section 111 as well as the second puncturing section 113 are roughly the same as the configuration of the first

repetition section 103. Accordingly, about the first puncturing section 111 as well as the second puncturing section 113, an explanation about the configuration is omitted. There will be explained about only operation in an operation explanation as describe later.

[0032]

Next, there will be explained about operation of the first repetition section 103. FIG.3 is a flowchart for explaining operation of the first repetition section 103. Firstly, in ST301, the control section 203 calculates increased the number of bits namely the total number of bits 'R' for repetition in accordance with an expression (1) from the number of bits 'N' per one frame stored in the parameter storage section 202 and the number of bits 'N0' before repetition.

$$R = N - N0 \quad (1)$$

[0033]

Next, in ST302, the control section 203 calculates the number of bits 'r1' for the first repetition. In order to perform repetition to the data while separating repetition into two stages in well-balanced condition, 'r1' is calculated in such a way of showing of an expression (2) with 'R' employed.

$$r1 = R/2 \text{ (rounding off less than a decimal point)} \quad (2)$$

[0034]

Next, in ST303, the control section 203 calculates

a first repetition interval 'X1' that means whether the control section 203 performs the first repetition in every how many bits in accordance with an expression (3).

$$X1 = N0/r1 \text{ (rounding off less than a decimal point)} \quad (3)$$

[0035]

Next, in ST304, the control section 203 performs compensation of 'r1', and 'X1'. This compensation is one causing the first repetition to be executed in accordance with a code rate to be performed according to expressions (4) to (6). Specifically, for instance, in the case where a code rate of data is 1/2, the first repetition is performed in every the number of bits to be multiples of 2, while in the case where a code rate of data is 1/3, the first repetition is performed in every the number of bits to be multiples of 3. Thus 'r1' and 'X1' are compensated in accordance with above described manner.

[0036]

Firstly, the control section 203 performs the remainder calculation showed in an expression (4).

$$\mathrm{mod}(X1 + m, C) = 0 \quad m \geqq 0 \quad (4)$$

Here, 'C' is an inverse number of a code rate of data, and this expression (4) is one for calculating the minimum 'm' causing the remainder to be '0'(zero) when 'X1 + m' is divided by 'C'. The control section 203 calculates a compensated value 'X1'' of 'X1' in accordance with an expression (5) while employing 'm' calculated

by this expression (4). According to this processing, 'X1' is compensated into 'X1''.

$$X1' = X1 + m \quad (5)$$

Further, the controller 203 calculates compensated value 'r1'' of 'r1' in accordance with an expression (6) while employing 'X1'' calculated by the expression (5). According to this processing, 'r1' is compensated into 'r1''.

$$r1' = N0/X1' \text{ (rounding off less than decimal point)} \quad (6)$$

[0037]

Subsequently, a value of a counter 'Ct' set in the control section 203 is added one by one from '1'(one). Then, processing of ST305 to ST310 is performed repeatedly over 'N0' times up to the state where the value of the counter 'Ct' becomes 'N0'. In ST306, the control section 203 performs the remainder calculation of an expression (7).

$$mod(Ct, X1') = b1 \quad (7)$$

Here, 'b1' is a parameter for setting whether the first repetition is started from how many numbers of bits of a frame. The 'b1' is set in the parameter storage section 202 beforehand.

[0038]

In ST306, in the case where the remainder of the division of dividing 'Ct' by 'X1'' becomes equal to 'b1', in ST307, the control section 203 sets the number of times

'n' of data output to '2'. in ST306, in the case where the remainder of the division of dividing 'Ct' by 'X1'' does not become equal to 'b1', in ST308, the control section 203 sets the number of times 'n' of data output to '1'.

[0039]

In ST309, the memory read/write section 204 reads the data stored in the input memory section 201 one bit by one bit to write to the output memory section 205 over 'n' times. Namely, concerning the bit set to 'n=2', the number of bits is increased.

[0040]

According to a processing-flow described-above, the first repetition of causing the number of bits to be increased for only the number of bits 'r1'' roughly half the number of total bits 'R' for the repetition is performed. Concerning the data after the first repetition, rearrangement of data is performed in accordance with the interleaving pattern in the interleaving section 104, subsequently the data is subjected to the second repetition in the second repetition section 105.

[0041]

Next, there will be described about operation of the second repetition section 105. FIG.4 is a flowchart for explaining operation of the second repetition section 105. Firstly, in ST401, the control section 203 within the second repetition section 105 calculates the number of bits 'r2' for the second repetition in accordance with

an expression (8) from the number of total bits 'R' for the repetition calculated by the first repetition section 103 and compensated number of bits 'r1'' for the first repetition.

$$r2 = R - r1' \quad (8)$$

[0042]

Next, in ST402, the control section 203 calculates a second repetition interval 'X2' that means whether the control section 203 performs the second repetition in every how many bits in accordance with an expression (9).

$$X2 = N1/r2 \text{ (rounding off less than a decimal point)} \quad (9)$$

Here, 'N1' is 'N1 = N0 + r1'', which represents the number of bits after the first repetition.

[0043]

Subsequently, a value of the counter 'Ct' set in the control section 203 is added one by one from '1'(one). Then, processing of ST403 to ST408 is performed repeatedly over 'N1' times up to the state where the value of the counter 'Ct' becomes 'N1'. In ST404, the control section 203 performs the remainder calculation of an expression (10).

$$\mathrm{mod}(Ct, X2) = b2 \quad (10)$$

Here, 'b2' is a parameter for setting whether the second repetition is started from how many numbers of bits of a frame. This 'b2' is set in the parameter storage section 202 arbitrarily.

[0044]

In ST404, in the case where the remainder of the division of dividing 'Ct' by 'X2' becomes equal to 'b2', in ST405, the control section 203 sets the number of times 'n' of data output to '2'. While, in ST404, in the case where the remainder of the division of dividing 'Ct' by 'X2' does not become equal to 'b2', in ST406, the control section 203 sets the number of times 'n' of data output to '1'.

[0045]

In ST407, the memory read/write section 204 reads the data stored in the input memory section 201 one bit by one bit to write to the output memory section 205 over 'n' times. Namely, concerning the bit set to 'n=2', the number of bits is increased.

[0046]

According to the processing-flow described-above, the second repetition is performed to the data after the first repetition. According to this processing, a repetition satisfying the total number of bits per one frame is performed.

[0047]

Next, there will be described concerning processing of the receiver side. In the receiver side, the first puncturing section 111 and the second puncturing section 113 perform inverse processing against the transmitter side, namely perform puncturing, to the bits increased

by the first repetition and the second repetition in the transmitter side. According to this processing, received data 117 is obtained. Specific operation is as follows.

[0048]

Firstly, there will be described about operation of the first puncturing section 111. FIG. 5 is a flowchart for explaining operation of the first puncturing section 111. The first puncturing section 111 performs processing for decreasing the bits increased in the second repetition section 105.

[0049]

In ST501, a first puncturing interval 'X2' that means whether the first puncturing is performed in every how many bits is set to the parameter storage section 202 in accordance with control data transmitted from the transmitter side. This 'X2' is equal to the second repetition interval 'X2'.

[0050]

Subsequently, the processing of ST502 to ST505 is performed repeatedly over 'N' times up to the state where a value of the counter 'Ct' set in the control section 203 is added one by one from '1'(one) to come into 'N'. Here, 'N' is 'N = N0 + r1' + r2', thus representing the number of bits after the second repetition, namely representing the number of bits per one frame. In ST503, the control section 203 performs the remainder calculation of an expression (11).

$$\mathrm{mod}(Ct, X2) = b2 \quad (11)$$

Here, 'b2' is equal to 'b2' which is employed when the second repetition is performed. The 'b2' is set to the parameter storage section 202 in accordance with the above control signal.

[0051]

Next, in ST504, the memory read/write section 204 reads data stored in the input memory section 201 one bit by one bit. Then, in the case where the remainder of the division of dividing 'Ct' by 'X2' does not become equal to 'b2', the memory read/write section 204 writes the read data to the output memory section 205 once. While in the case where the remainder of the division of dividing 'Ct' by 'X2' becomes equal to 'b2', the memory read/write section 204 abolishes the read data.

[0052]

According to the processing-flow described-above, the first puncturing is performed to the bits increased by the second repetition. Concerning the data after the first puncturing, an inverse rearrangement against the rearrangement of data performed in the interleaving section 104 is performed in the deinterleaving section 112. Subsequently, the data is subjected to the second puncturing in the second puncturing section 113.

[0053]

Next, there will be described operation of the second puncturing section 113. FIG.6 is a flowchart for

explaining operation of the second puncturing section 113. The second puncturing section 113 performs processing for decreasing the bits increased by the first repetition section 103.

[0054]

Firstly, in ST601, a second puncturing interval 'X1'' that means whether the second puncturing is performed in every how many bits is set to the parameter storage section 202 in accordance with the above control data. This 'X1'' is equal to the compensated first repetition interval 'X1''.

[0055]

Subsequently, the processing of ST602 to ST605 is performed repeatedly over 'N1' times up to the state where a value of the counter 'Ct' set in the control section 203 is added one by one from '1'(one) to come into 'N1'. This 'N1' is equal to 'N1' which is employed in the second repetition to be set to the control section 203 in accordance with the above control signal.

In ST603, the controller 203 performs the remainder calculation of an expression (12).

$$mod(Ct, X1') = b1 \quad (12)$$

Here, 'b1' is equal to the 'b1' employed when the first repetition is performed, to be set to the parameter storage section 202 in accordance with the above control signal.

[0056]

Next, in ST604, the memory read/write section 204 reads the data stored in the input memory section 201 one bit by one bit. Then in the case where the remainder of the division of dividing 'Ct' by 'X1'' does not become equal to 'b1', the memory read/write section 204 writes the read data to the output memory section 205 once. While in the case where the remainder of the division of dividing 'Ct' by 'X1'' becomes equal to 'b2', the memory read/write section 204 abolishes the read data.

[0057]

According to the processing-flow described-above, the second puncturing is performed to the bits increased by the first repetition. The data after the second puncturing is subjected to error correction by Viterbi decoding and so forth in the error correction decoding section 114, before being decoded in the decoding section 115. According to this processing, received data 117 is obtained.

[0058]

Next, there will described the circumstances in detail in which transmitted data is subjected to repetition and interleaving due to the coding processing apparatus 100 of the present embodiment while employing FIG.7. Now, data outputted from the coding section 101 is taken to be {D1, D2, D3, D4}. The data is subjected to error correction coding processing with "code rate = 1/2" in the error correction coding section 102. As

a result, in cases where 'D1' becomes 'd1', and 'd2', 'D2' becomes 'd3', and 'd4', 'D3' becomes 'd5', and 'd6', and 'D4' becomes 'd7', and 'd8', data inputted to the first repetition section 103 becomes data of 8 bits of {d1, d2, d3, d4, d5, d6, d7, d8}. Further, the number of bits per one frame is 12 bits.

[0059]

In the first place, the first repetition section 103 performs the first repetition in accordance with processing-flow of FIG.3. Firstly, in ST301 to ST303, 'R', 'r1', and 'X1' are calculated in accordance with above expressions (1) to (3). Following result is obtained.

$$R = N - N0 = 12 - 8 = 4 \quad (13)$$

$$r1 = R/2 = 4/2 = 2 \quad (14)$$

$$X1 = N0/r1 = 8/2 = 4 \quad (15)$$

[0060]

Next, in ST304, 'r1' and 'X1' are compensated in accordance with above expressions (4) to (6). Now, since the code rate of the error correction coding processing is '1/2', 'C' becomes 'C=2'. Consequently, above expression (4) is calculated as following way.

$$mod(X1 + m, C) = 0$$

$$mod(4 + m, 2) = 0$$

$$\therefore m = 0 \quad (16)$$

[0061]

Here, since 'm' is 'm=0', following result is

obtained in accordance with above expressions (5), and (6).

$$X1' = X1 = 4 \quad (17)$$

$$r1' = r1 = 2 \quad (18)$$

[0062]

Next, in ST305 to ST310, the number of bits of corresponding bits is increased in accordance with the above expression (7) up to the state where 'Ct' becomes 'N0' from '1'. Now, in the case where 'b1' is set to "b1=2", in accordance with the above expression (7), the number of bits of 'd2' to be data of the second bit as well as the number of bits of 'd6' to be data of the sixth bit are increased, thus the first repetition is performed. Consequently, the data after the first repetition becomes {d1, d2, d2, d3, d4, d5, d6, d6, d7, d8} as showed in FIG.7. Further, the data showed by underline in FIG.7 are ones whose number of bits is increased due to repetition.

[0063]

Next, concerning the data after the first repetition, rearrangement of data is performed in accordance with interleaving pattern "10[5[3×2]×2]" in the interleaving section 104. As a result, the data after interleaving becomes {d1, d4, d7, d2, d6, d2, d5, d8, d3, d6}.

[0064]

Next, the second repetition section 105 performs the second repetition to the data after interleaving in

accordance with the processing-flow of FIG.4. Firstly, in ST401 to ST402, in accordance with the above expressions (8) to (9), 'r2' and 'X2' are calculated as follows:

$$r2 = R - r1' = 4 - 2 = 2 \quad (19)$$

$$X2 = N1/r2 = 10/2 = 5 \quad (20)$$

[0065]

Next, in ST403 to ST408, the number of bits of corresponding bits is increased in accordance with the above expression (10) up to the state where 'Ct' becomes 'N1' from '1'. Now, in the case where 'b2' is set to 'b2=2', in accordance with the above expression (10), the number of bits of 'd4' to be data of the second bit as well as the number of bits of 'd5' to be data of the seventh bit are increased, thus the second repetition is performed. Consequently, the data after the second repetition becomes {d1, d4, d4, d7, d2, d6, d2, d5, d5, d8, d3, d6} as showed in FIG.7.

[0066]

Thus, according to the coding processing apparatus and the decoding processing apparatus of the present embodiment, since repetition is performed at two stages before and after interleaving, it is possible to prevent that the bits increased due to repetition exist while being partial to one position within a frame. For that reason, it is possible to improve a bit error rate characteristic when the receiver side performs error correction in comparison with the conventional coding

processing apparatus and the conventional decoding processing apparatus in which repetition is performed only once before interleaving.

[0067]

It should be noted that, in the above specific example, in the case where the interleaving pattern is 10[5[3×2]×2], an effect of the present embodiment becomes the most remarkable. However, even though an interleaving pattern is another one, it can be observed that the present embodiment has an effect. Furthermore, in the above specific example, there is described the embodiment while setting various kinds of parameters arbitrarily. However, it is nothing but one example. Accordingly, the effect of the present embodiment is not observed while being limited from values of these parameters, but the effect of the present embodiment is observed even though parameters adopt another values.

[0068]

(Embodiment 2)

Next, there will be described an embodiment 2 of the present invention. FIG.8 is a block diagram illustrating a configuration of a coding processing apparatus and a decoding processing apparatus according to the embodiment 2 of the present invention. In a coding processing apparatus 800, the configuration of the coding processing apparatus 800 is one in which the second repetition section 105 is removed from the coding

processing apparatus 100 of the embodiment 1. Another configuration and operation of respective sections are the same as that of coding processing apparatus 100.

[0069]

Consequently, in a transmitter side, the data which is subjected to the error correction coding processing in the error correction coding section 102 is subjected to a first repetition by the first repetition section 103 in which 'r1' calculated in ST302 at the processing-flow showed in FIG.3 described-above is taken to be 'r1=R'. The data after the first repetition is rearranged in the interleaving section 104. Subsequently, the data is subjected to predetermined modulation processing and predetermined radio processing and so forth, before being transmitted from the transmission antenna 107.

[0070]

On the other hand, in a decoding processing apparatus 810, the configuration of the decoding processing apparatus 810 is one in which the first puncturing section 111 is removed from the decoding processing apparatus 110 of the embodiment 1. Another configuration and operation of respective sections are the same as that of decoding processing apparatus 110.

[0071]

Consequently, in the receiver side, data to which inverse rearrangement against the interleaving of the

transmitter side is performed in the deinterleaving section 112 is subjected to inverse second puncturing against the first repetition in accordance with the processing-flow showed in FIG.6 described above by the second puncturing section 113. The data after the second puncturing is subjected to the error correction by Viterbi decoding and so forth in the error correction decoding section 114.

[0072]

Thus, according to the coding processing apparatus and the decoding processing apparatus of the present embodiment, the repetition is performed while determining increased bits in accordance with the code rate such that in the case where the code rate of the data is '1/2', the increased bits are determined in every the number of bits of multiples of 2, and such that in the case where the code rate of the data is '1/3', the increased bits are determined in every the number of bits of multiples of 3. Consequently, according to the coding processing apparatus and the decoding processing apparatus of the present embodiment, it is possible to prevent that the repetition is performed repeatedly to a plurality of data after error correction coding, which are generated from the same data before error correction coding, caused by error correction coding processing. Thus, according to the coding processing apparatus and the decoding processing apparatus of the present embodiment, since

it is possible to enhance an effect of the error correction coding, it is possible to improve a bit error rate characteristic when the receiver side performs error correction in comparison with the conventional coding processing apparatus and the conventional decoding processing apparatus.

[0073]

(Embodiment 3)

Next, there will be described an embodiment 3 of the present invention. FIG.9 is a block diagram illustrating a configuration of a coding processing apparatus and a decoding processing apparatus according to the embodiment 3 of the present invention. In a coding processing apparatus 900, the configuration of the coding processing apparatus is one in which the first repetition section 103 is removed from the coding processing apparatus 100 of the first embodiment. Another configuration and operation of respective sections are the same as that of the coding processing apparatus 100.

[0074]

Consequently, in the transmitter side, the data which is rearranged in the interleaving section 104 is subjected to a second repetition by the second repetition section 105 in which 'r2' calculated in ST401 at the processing flow showed in FIG.4 described-above is taken to be 'r2=R'. The data after the second repetition is

subjected to predetermined modulation processing and predetermined radio processing and so forth, before being transmitted from the transmission antenna 107.

[0075]

On the other hand, in a decoding processing apparatus 910, the configuration is one in which the second puncturing section 113 is removed from the decoding processing apparatus 110 of the embodiment 1. Another configuration and operation of respective sections are the same as that of the decoding-coding processing apparatus 110.

[0076]

Consequently, in the receiver side, a signal received by the reception antenna 116 is subjected to predetermined radio processing and predetermined demodulation processing and so forth. Subsequently, the received signal is subjected to a first puncturing which is inverse processing against the second repetition in accordance with the processing- flow showed in FIG.5 described-above by the first puncturing section 111. Concerning the data after the first puncturing, inverse rearrangement against the interleaving of the transmitter side is performed in the deinterleaving section 112.

[0077]

Thus, according to the coding processing apparatus and the decoding processing apparatus of the present embodiment, since the repetition is performed after

interleaving, it is possible to prevent that the bits increased due to repetition exist while being partial to one position within a frame. Consequently, according to the coding processing apparatus and the decoding processing apparatus of the present embodiment, it is possible to improve a bit error rate characteristic when the receiver side performs error correction in comparison with the conventional coding processing apparatus and the conventional decoding processing apparatus in which repetition is performed before interleaving.

[0078]

The coding processing apparatus and the decoding processing apparatus according to the embodiments 1 to 3 described-above are applicable to a communication terminal apparatus and a base station apparatus such as a mobile station apparatus in a CDMA radio communication system. In the case of application, since the base station apparatus and the communication terminal apparatus are equipped with the coding processing apparatus and the decoding processing apparatus, which can lower the bit error rate, it is possible to scheme improvement of communication quality.

[0079]

It should be noted that, in the explanation of the above embodiments 1 to 3, for the sake of convenience, there is explained the embodiments while separating the apparatus of the present invention into the transmitter

and the receiver. However, a radio communication apparatus in a CDMA radio communication system also can be provided with both of the transmitter and the receiver.

[0080]

[Effects of the Invention]

As described-above, according to the present invention, it is possible to scheme improvement of communication quality because resistibility to a burst error in a propagation path becomes high.

[BRIEF DESCRIPTION OF THE DRAWINGS]

[FIG.1] A block diagram illustrating a configuration of a coding processing apparatus and a decoding processing apparatus according to an embodiment 1 of the present invention.

[FIG.2] A block diagram illustrating a configuration of a repetition section and a puncturing section according to the embodiment 1 of the present invention.

[FIG.3] A flowchart for explaining operation of a first repetition section according to the embodiment 1 of the present invention.

[FIG.4] A flowchart for explaining operation of a second repetition section according to the embodiment 1 of the present invention.

[FIG.5] A flowchart for explaining operation of a first puncturing section according to the embodiment 1 of the present invention.

[FIG.6] A flowchart for explaining operation of a second puncturing section according to the embodiment 1 of the present invention.

[FIG.7] A view showing data arrangement in the case where repetition is performed with the coding processing apparatus employed according to the embodiment 1 of the present invention.

[FIG.8] A block diagram illustrating a configuration of a coding processing apparatus and a decoding processing apparatus according to the embodiment 2 of the present invention.

[FIG.9] A block diagram illustrating a configuration of a coding processing apparatus and a decoding processing apparatus according to the embodiment 3 of the present invention.

[FIG.10] A block diagram illustrating a configuration of a conventional coding processing apparatus and decoding processing apparatus.

[FIG.11] A view showing data arrangement in the case where repetition is performed with the conventional coding processing apparatus employed.

[Description of the Symbols]

103 First repetition section

104 Interleaving section

105 Second repetition section

111 First puncturing section

112 Deinterleaving section

113 Second puncturing section

201 Input memory section

203 Control section

204 Memory read/write section

205 Output memory section